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THOMAS, KAYDEN, HORSTEMEYER & RISLEY LLP
600 GALLERIA PARKWAY, 15TH FLOOR
ATLANTA, GA 30339

EXAMINER	
TRAN, BINH X	

ART UNIT	PAPER NUMBER
1792	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/247,974	YING ET AL.	
	Examiner	Art Unit	
	Binh X. Tran	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-17, 19, 20, 22-25* is/are allowed.

6)☐ Claim(s) *1-15, 18, 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to the petition decision to withdraw the holding of abandonment mailed on 02-19-2008. The petition is granted and the holding of the abandonment is withdrawn (See petition decision for further detail).

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11-28-2000 has been entered.

Specification

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The claim 7 and 21, the examiner is unable to find the proper support for the limitation “BOE solution of 10:1 or 50:1” in the specification. The examiner clearly recognizes that applicants discloses to use buffer oxide etch (BOE). However, applicants fail to disclose the specific ratio or provide proper antecedent basis regarding the ratio (10:1 or 50:1) of BOE solution in the specification.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 3, 7-8, 10, 11, 14, 15, 18, 21, 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites the limitation "the SAC process" in line 4. There is insufficient antecedent basis for this limitation in the claim.

In claim 7 and 21, the limitation "BOE solution of 10:1 or 50:1" is vague and indefinite. It is unclear from the claim what specific ratio of the BOE solution that applicants wish to claim.

Claim 8 recites the limitation "said exposed top corners" in line 9. There is insufficient antecedent basis for this limitation in the claim.

Claim 10 recites the limitation "the partially exposed top corners" in lines 8-9. There is insufficient antecedent basis for this limitation in the claim.

Claim 11 recites the limitation "the partially exposed top corners" in line 9. There is insufficient antecedent basis for this limitation in the claim.

Claim 14 recites the limitation "said spacer" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 15 recites the limitation "said deposited of PE-oxide or PE-TEOS" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 15 recites the limitation "said conducting line pattern" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 18 recites the limitation "the SAC process" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 26 recites the limitation "said conducting line pattern" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1-4, 12, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsueh et al. (US 5,990,009) in view of Lee (US 5,663,092).

Respect to claim 1, Hsueh discloses a method of filling gaps between a pattern of interconnection lines forming wring structure on a semiconductor substrate, said

interconnect lines having a top surface further having sidewalls (See Fig 5F) comprising the steps of:

providing a semiconductor substrate said substrate having a surface (Fig 5F);

creating a network of interconnect line on said surface of said substrate, whereby said interconnect lines are separated by holes (120) having bottoms between said interconnect lines (Fig 5F, col. 4 lines 42-67);

depositing a first layer of dielectric (114) having a surface over said interconnection lines wiring structure (Fig 5G, col. 5 lines 4-10);

depositing a second layer of dielectric (116) having a surface over said first dielectric (114) (Fig 5H);

etching said second layer of dielectric layer (116) creating exposed portions of said first layer of dielectric (Fig 5I-5J, col. 5 lines 28-65);

performing an etch back of said first dielectric layer (Fig 5J, col. 5 lines 56-65)

depositing a layer of oxide (118) over said etched second layer of dielectric (116) thereby including said exposed portion of said first dielectric layer (114)(Fig 4, col. 5 line 65 to col. 6 lines 18).

Hsueh fails to disclose that the holes have bottom between the interconnect lines thereby leaving the surface of the substrate partially exposed over said bottoms of said holes between interconnection lines. Lee teaches the holes between the interconnection lines (gate) thereby leaving the surface of the substrate partially exposed over said bottoms of said holes between interconnection lines (See Fig 6). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Hsueh

in view of Lee by leaving the surface of the substrate partially expose over the bottoms of the holes because it helps to expose source and drain region (118/119) of the substrate.

Hsueh also fails to disclose deposited a second layer of the dielectric having a surface over said etched back first layer of dielectric. However, Hsueh clearly discloses deposit a second dielectric (116) over the first dielectric (114) (Fig 5H-5I). Lee teaches to etch back the first dielectric layer (120). Lee further teaches to deposit a second layer dielectric layer on the etched back first layer of dielectric (120) to fill the holes in between the interconnection lines (Fig 6-7). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Hsueh by etching back the first dielectric layer and deposit a second dielectric layer over the etched back first dielectric layer because it helps to remove extra portions of the first dielectric layer and provide a material to fill the holes between interconnection holes.

Respect to claims 2-4, Hsueh discloses the interconnections lines contain a lower layer of conducting material including polysilicon (110B) and an upper layer of silicon nitride (112) and said interconnections line is applied during the self-aligned contact process (col. 3 lines 54 to col. 4 line 30, Fig 5E-5F). Respect to claim 12, Hsueh disclose etching the second layer of dielectric (116) removing the second layer of dielectric in its totality except where said second layer of dielectric (116) forms spacers on the sidewalls of the interconnect lines (Fig 5J).

Respect to claim 15, Hsueh teaches to planarize the PE oxide layer (118) to an appropriate thickness (col. 5 line 65 to col. 6 lines 11). Hsueh is silent whether the

planarization is proceeded down to the plane of the top surface of the conducting line pattern.

In an interconnect method, Lee discloses planarization is proceeded down to the plane of the top surface of the conducting line pattern thereby completing the process of creating a high-aspect ratio pattern of conducting lines said conducting lines being separated with an intra-layer dielectric (col. 5 line 38-41).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Hsueh in view of Lee by planarizing down to the plane of the top surface of the conducting line pattern because planarization will remove extra portion and smooth the surface of a dielectric layer.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsueh and Lee as applied to claims 1-4, 12, 15 above, and further in view of Yao (US 5,814,564)

Respect to claim 5, Hsueh and Lee are silent whether the dielectric contains high density plasma oxide. However, Hsueh clearly discloses the first dielectric layer is plasma oxide (col. 5 lines 4-10). Yao teaches to use plasma oxide dielectric including high density plasma oxide (col. 4). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Hsueh and Lee by using high density plasma oxide for the dielectric because equivalent and substitution of one for the other would produce an expected result.

10. Claim 9, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsueh and Lee as applied to claims 1-4, 12, 15 above, and further in view of Lu (US6,479,341).

Respect claim 9, Hsueh and Lee fail to disclose the second layer of dielectric is depositing a layer Si_3N_4 using PECVD technology at a temperature of about 400 ° whereby said layer of Si_3N_4 is deposited to a thickness between about 1000-2000 angstroms. However, Hsueh clearly disclose to deposit second dielectric layer using CVD process (col. 5 lines 28-40). Lu discloses to deposit a second dielectric layer comprises Si_3N_4 using PECVD to a temperature between 400-700 °C at a thickness between 500-2,000 angstroms (read on applicants' range). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Hsueh and Lee in view of Lu by depositing Si_3N_4 using PECVD at said temperature and thickness ranges because it helps to create the spacers to protect the interconnect lines (i.e. gate structures)

Claims 13 differ from Hsueh and Lee by further specifying CHF_3 as the etchant gas for silicon nitride at the flow rate of 15 sccm, pressure of 15 mtorr, rf power density of about 700 watts with no magnetic field and ambient wafer temperature of 15 °C. Lu discloses the use of CHF_3 as the etchant gas for silicon nitride layer with no magnetic field applied (col. 4 lines 1-15). Claim 13 further differ from Lu by the specific value of etchant gas flow rate, gas pressure, rf power density. It would have been prima facie obvious to employ any of a variety of etchant gas flow rate, gas pressures, rf power densities including those claimed by applicant. These are all well known variable

in the plasma etching art which are known to effect both the rate and quality of the plasma etching process. Further, the selection of particular values for these variables would simply involve routine experimentation and the determination of workable ranges in not considered inventive.

Allowable Subject Matter

11. Claim 6-8, 10-11, 14 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

12. Claims 16-17, 19, 20, 22-25 are allowed.

13. Claim 18, 21, 26 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

The following is a statement of reasons for the indication of allowable subject matter:

Respect to claims 6-7, the cited prior arts fail to disclose or suggest etch back the first dielectric layer using buffer oxide etch thereby forming a layer of first dielectric having a surface on the bottom of the holes that separate said interconnect lines thereby further forming deposit of said first dielectric, said deposits partially overlaying the top surfaces of said interconnect lines thereby creating exposed top corners of said interconnect lines, said top corners being located at intersects between said sidewalls of said interconnect lines and said top surface.

Respect to claim 8, the cited prior arts fail to disclose or suggest depositing a layer of silicon nitride, said deposition covering the surface of said layer of first dielectric

on the bottom of said hole between said interconnect lines thereby further covering the surface of said first dielectric partially overlaying the top surfaces of said interconnect lines thereby furthermore covering the surface of said exposed top corners of said interconnect lines.

Respect to claim 10, the cited prior arts fail to disclose or suggest depositing a second layer of dielectric is depositing a layer of aluminum oxide said deposition covering the surface of said layer of first dielectric on the bottom of said holes separating said interconnect lines thereby further covering the surface of said first dielectric partially overlaying the top surfaces of said interconnect lines thereby furthermore covering the surface of the partially exposed top corners of said interconnect lines.

Respect to claim 11, the cited prior arts fail to disclose or suggest depositing a second layer of dielectric is depositing a layer of dielectric material said deposition covering the surface of said layer of first dielectric on the bottom of the holes separating said interconnect lines thereby further covering the surface of said first dielectric partially overlaying the top surfaces of said interconnect lines thereby furthermore covering surface of the partially exposed top corners of said interconnect lines.

Respect to claim 14, the cited prior arts fail to disclose or suggest said depositing a layer of oxide is depositing a layer of PE-oxide or PE-TEOS over said spacers on said sidewalls of said interconnect lines thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said layer of first dielectric on the bottom of the holes between said interconnect lines thereby furthermore depositing a layer of PE-oxide or PE-TEOS

over said first dielectric partially overlaying the top surfaces of said interconnect lines thereby furthermore depositing a layer of PE-oxide or PE-TEOS over the partially exposed top corners of said interconnect lines.

Respect to claim 16, the cited prior arts fail to disclose or suggest depositing a layer of PE-oxide or PE-TEOS over said spacers on the sidewalls of said interconnect lines thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said layer of first dielectric on the bottom of the holes between said interconnect lines thereby furthermore depositing a layer of PE- oxide or PE-TEOS over said first dielectric partially overlaying the top surfaces of said interconnect lines thereby furthermore depositing a layer of PE-oxide or PE-TEOS over the partially exposed top corners of said interconnect lines in combination with the buffer oxide etch of the first dielectric layer.

Response to Arguments

14. The applicant's argument regarding the previous 35 USC 112 , 2nd paragraph rejection is persuasive. Thus, the previous ground of rejection under 35 USC 112, 2nd paragraph has been withdrawn. However, upon further consideration, a new ground of rejection is made as discussed above.

Applicant's arguments, see pages 10-19, filed 11-06-2000, with respect to the previous ground of rejection of claims 1-5 under 35 USC 103(a) using Parat et al. (US 5,731,242) as one of the reference been fully considered and are persuasive.

Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made as discussed above.

The applicant's argument with respect to claim 6, 8, 10-11, 14, 16 is persuasive. Thus, the 35 USC 103(a) ground of rejection have been withdrawn (See allowable subject matter section above for further detail).

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh X. Tran whose telephone number is (571)272-1469. The examiner can normally be reached on Monday-Thursday and every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Binh X Tran
Primary Examiner
Art Unit 1792

/Binh X Tran/
Primary Examiner, Art Unit 1792